Abstract

In one example embodiment, a high-speed parallel-data communication approach transfers digital data in parallel from a first module to a second module over a communication channel including a plurality of parallel data-carrying lines and a clock path. The parallel bus lines are arranged in a plurality of groups, each of the groups including a plurality of data-carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried from the first module to the second module. The sets of data are concurrently transferred using the groups of lines of the parallel bus, and at the second module and for each group, the transferred digital data is synchronously collected via the clock signal for the group. At the second module, the data collected for each group is aligned. By grouping the bus lines in groups with each group having its own clock domain, skew across clock-domain groups is tolerated and overcome by processing the data and the skew first within each clock domain group, and then between groups.